Plasma Assisted Low Temperature Semiconductor Wafer Bonding

Zum Seminar Optoelektronik - Wafer-Fusing

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Inhaltsverzeichnis

Literatur

[Don] Donato Pasquariello. Plasma Assisted Low Temperature Semiconductor Wafer Bonding.

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1 Vorwort

[Don]ff.

Für effiziente Kavitätsfotodetektoren muß zumindest einer der beiden erforderlichen Spiegel ein Reflexionsvermögen von mehr als 99,5% aufweisen. Diese Anforderung zu erfüllen, ist bei langwelligen Fotodetektoren schwieriger als bei kurzwelligen, weil diese hochreflektierenden Spiegel nur schwierig durch den gleichen Schritt des epitaktischen Wachstums gebildet werden können wie die langwellige aktive Zone.

Da epitaktisch gewachsene Spiegel häufig kein ausreichend hohes Reflexionsvermögen zeigen, werden Fotodetektoren durch Wafer-Fusing des oberen und des unteren Spiegels an der aktiven Zone gebildet.

Diese Wafer-Fusion ist ein Verfahren, mit dem Werkstoffe verschiedener Gitterkonstante atomar miteinander verbunden werden durch Aufbringen von Druck und Wärme, um eine echte physikalische Bindung zu erzeugen.

Damit dient das Wafer-Fusing einer oder beider Spiegel an die aktive Zone zur Steigerung des Reflexionsvermögens, welches der eine Spiegel oder beide Spiegel aufweisen müssen.

2 Originaltext

Dokument nächste Seite folgend.

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Plasma Assisted Low Temperature Semiconductor Wafer Bonding

BY

DONATO PASQUARIELLO

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Donato Pasquariello

Plasma Assisted Low Temperature Semiconductor Wafer Bonding

Dissertation in Materials Science to be publicly examined in lecture room Siegbahnsalen at the Ångström Laboratory, Uppsala University, on April 20, 2001 at 10.15 a.m., for the Degree of Doctor of Philosophy.

Abstract
Pasquariello, D. 2001. Plasma Assisted Low Temperature Semiconductor Wafer Bonding. Acta Universitatis Upsaliensis. *Comprehensive Summaries of Uppsala Dissertations from the Faculty of Science and Technology* 621. 37 pp. Uppsala. ISBN 91-554-4993-X.

Direct semiconductor wafer bonding has emerged as a technology to meet the demand for additional flexibility in materials integration. The applications are found in microelectronics, optoelectronics and micromechanics. For instance, wafer bonding is used to produce silicon-on-insulator (SOI) wafers. Wafer bonding is also interesting to use for combining dissimilar semiconductors, such as Si and InP, with different dictated optical, electronic and mechanical properties. This enables a completely new freedom in the design of components and systems, e.g. for high performance optoelectronic integrated circuits (OEIC). Although wafer bonding has proved to be a useful and versatile tool, the high temperature annealing that is needed to achieve reliable properties sometimes hampers its applicability. Therefore, low temperature wafer bonding procedures may further qualify this technology.

In the present thesis, low temperature wafer bonding procedures using oxygen plasma surface activation have been studied. A specially designed fixture was adopted enabling *in situ* oxygen plasma wafer bonding. Oxygen plasma surface activation was seen to indeed yield high Si-Si bonding-strength at low temperatures. Here, the optimisation of the plasma parameters was shown to be the key to improved results. Furthermore, dependence of wafer bonded Si p-n junctions on the annealing temperature was investigated.

InP-to-Si wafer bonding is also presented within this thesis. High temperature annealing was seen to induce severe material degradation. However, using oxygen plasma assisted wafer bonding reliable InP-to-Si integration was achieved already at low temperature, thereby circumventing the problems associated with the lattice and thermal mismatch that exist between these materials. As a result, low temperature InP-based epitaxial-layer transferring to Si could be presented. Finally, high-quality SiO_2 insulator on InP and Si was realised at low temperatures.

It is concluded that low temperature oxygen plasma assisted wafer bonding is an interesting approach to integrate dissimilar materials, for a wide range of applications.

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List of papers included in this thesis

This thesis is based on the following papers, which will be referred to in the text by their Roman numerals:

I. *"Surface energy as a function of self-bias voltage in oxygen plasma wafer bonding"*
D. Pasquariello, M. Lindeberg, C. Hedlund and K. Hjort
Sensors & Actuators, **A82** pp. 239-244 (2000)

II. *"Oxidation and induced damages in oxygen plasma in situ wafer bonding"*
D. Pasquariello, C. Hedlund and K. Hjort
Journal of the Electrochemical Society, **147** pp. 2699-2703 (2000)

III. *"Mesa-Spacers: enabling non-destructive measurements of surface energy in room temperature wafer bonding"*
D. Pasquariello and K. Hjort
Journal of the Electrochemical Society, **147** pp. 2343-2346 (2000)

IV. *"Evaluation of InP to Si heterobonding"*
D. Pasquariello, M. Camacho, K. Hjort, L. Dozsa and B. Szentpali
Material Science & Engineering B **80** pp. 134-137 (2001)

V. *"Crystalline defects in InP-to-Si direct wafer bonding"*
D Pasquariello, M. Camacho, F. Ericsson and K. Hjort
Accepted for publication in Japanese Journal of Applied Physics (2001)

VI. *"Low temperature fabrication of InP and Si MOS structures: using oxygen plasma wafer bonded thermally grown SiO_2 as insulator material"*
D. Pasquariello and M. Forsberg
Submitted to IEEE Transactions of Electron Devices

VII. *"Low temperature InP-based epitaxial layer transferring using oxygen plasma wafer bonding"*
D. Pasquariello, M. Karlsson and K. Hjort
Manuscript

VIII. *"Point Defects Generated by Direct Wafer Bonding of Silicon"*
L. Dozsa, B. Szentpali, D. Pasquariello and K. Hjort
Submitted to Journal of Electronic Materials

Author's contribution

Paper I-VI: major part of planning, experimental work, evaluation, and all writing.
Paper VII: part of planning, experimental work and evaluation
Paper VIII: part of planning, minor part of experimental work and evaluation.

List of papers not included in this thesis

A. *"Fabrication of tunable InP/air-gap Fabry-Perot cavities by selective etching of InGaAs sacrificial layers"*
N. Chitica, J. Dalaiden, J. Bentell, J. Andre, M. Strassner, S. Greek, D. Pasquariello, M. Karlsson, R. Gupta, K. Hjort
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B. *"InP based Micro Opto Electro Mechanics"*
D. Pasquariello, M. Karlsson, S. Greek, C. Hedlund, R. Gupta, K. Hjort
MicrostructureWorkshop '98, Uppsala, Sweden March 24-25, 1998, pp.201-12

C. *"Polymide based GaAs micromachined millimetre wave structures"*
A.Muller, S. Iordanescu, I. Petrini, V. Avramescu, G. Simion, D. Vasilache, V. Badilita, D. Dascalu, G. Konstantinidis, R. Marcelli, G Bartolucci, K. Hjort, D. Pasquariello, K. Hjort
Journal of Micromechanics and Microengineering, **10**, p.130-5, (2000)

D. *"Demands and solutions for an InP based micromechanically tunable WDM photodetector"*
K. Hjort, S. Greek, R. Gupta, D.Pasquariello, N. Chitica, K. Streubel, C. Seassal, J.-L. Leclerq, P. Viktorovitch, T. Benyattou, A. Dehe, J. Peerlings, J. Pfeiffer, P. Meissner, R. Riemenschneider, H. L. Hartnagel, D. D. Mongardien, O. Sahlén.
MOEMS'97, Int. Conf. On Optical MEMS and their Appl.(Nara, Japan, Nov. 18-21,1997) pp. 344-351

CONTENTS

PREFACE

The major part of the work in this thesis was carried out at the Department of Materials Science, The Ångström Laboratory, Uppsala University, within the competence centre for surface & microstructure technology (SUMMIT), financially supported by the Swedish Board for Industrial and Technological Development (NUTEK).

I would like to thank all the people that have encouraged and supported this work during the years. I would like to mention all of you that 'directly or indirectly' have made this work possible, the list would be very long, therefore I simply say –Thank You! Especially though I want to express my sincere gratitude to:

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Uppsala, March 2001

Donato Pasquariello

1. INTRODUCTION

Silicon (Si) is by far the most frequently used material in the fast growing microelectronic industry. Microelectronics is today one the world's biggest industries. The tendency in production of integrated circuits (ICs) moves towards shrinking component dimensions and increased complexity. The number of insulting layers and interconnects levels keep increasing. Silicon has also been adapted for purposes beyond purely electronic application, such as microelectromechanical systems (MEMS). Despite silicon's vast success III-V compound semiconductors has an unchallenged position in optoelectronic applications. Gallium arsenide (GaAs) and indium phosphide (InP) based material offers several advantages over Si. These advantages include direct bandgap, facilitating emission and absorption of light, and high mobility, thereby finding applications in high-speed devices. InP and its lattice match materials $In_{1-x}Ga_xAs_yP_{1-y}$ has received special attention since they cover the low dispersion and minimum loss wavelength of optical fibers. Therefore, they are widely used as active parts of receivers (detectors) and emitters (lasers) in optical fiber networks.

The technological progress in the field of semiconductor devices has sometimes pushed the achievements of each material system to its outermost limits. As system and device designer seeks for further improvement it may be found that the optimal solutions do not reside within one material but in a combination of disparate material, each having it unique properties concerning mechanical strength, optical emission and absorption, thermal and electrical conductivity. Combining III-V compound semiconductors with Si yields a whole new spectrum of design flexibility. The integration is interesting both for combining the unique properties into a single device and also to integrate e.g. optoelectronic components with advanced Si circuitry for the realization of optoelectronic integrated circuits (OEICs). However, heteroepitaxial growth as way of integrating dissimilar semiconductors is hampered by the lattice mismatch. Direct semiconductor wafer bonding has therefore emerged as an interesting alternative.
Direct Semiconductor Wafer Bonding by 'definition' means the joining of two atomically smooth and clean semiconductor surfaces at room temperature. No constrain on lattice matching exists and after joining the two wafer surfaces, the bonded pairs are annealed at a high temperature to ensure the formation of strong bonding. With proper procedure the bonded interface can achieve bulk strength.

Pioneering work in 'Direct Semiconductor Wafer Bonding', which will simply be referred to as wafer bonding through out this thesis, was done at Toshiba and IBM in the mid 80' as a substitute for thick epitaxial growth of Si and to realise SOI (silicon-on-insulator) material. Recently IBM committed itself to massproduction on SOI substrates and all of the leading IC manufactures have well-developed programs

for use of SOI wafers. The two front run contenders for producing SOI wafers are SIMOX, which will initially be used by IBM, and the direct wafer bonding. However, along with its maturation and introduction of layer splitting technologies, the direct wafer bonding approach is gaining terrain. Industry experts expect SOI to grow to greater than 50 % of the bulk wafer market by 2008, producing an $8 billion market for SOI wafers.
Although the main driving force for development of wafer bonding has been production of SOI wafers, several other high potential applications of wafer bonding have emerged in e.g microelectromechanical systems (MEMS) and as a way of integrating dissimilar crystalline materials.

While most other routine semiconductor processes have standardised and well characterised parameters more work is needed in this area for the relatively ‘young’ field of wafer bonding. To reach sufficient level of maturity wafer bonding procedures need to be optimised and standardised according to the application. Also, wafer bonding requires a high-temperature annealing step after the room temperature joining, to ensure the formation of a strong and uniform bonding. This high temperature annealing is sometimes incompatible with many applications and it may cause material degradation, especially when bonding thermally mismatched materials. All the way back to the pioneering days, low temperature wafer bonding procedures have been highly desired.

Within this thesis the annealing temperature in wafer bonding is the essence and the major work is focused on reducing it. This would further launch wafer bonding as a competitive technology and enable a wider use of it. The effect of annealing temperature on wafer bonded Si p-n junction is analysed. Most of the papers concentrate on the use of oxygen plasma surface activation as a way of achieving reliable low temperature wafer bonding procedures. A nonintrusive method to measure the bond-strength at room temperature has been developed. Finally, the applicability of wafer bonding as a tool to the integrate dissimilar material system InP and Si is presented and discussed.

2. SEMICONDUCTOR WAFER BONDING

In this section a brief introduction to wafer bonding is given and a ‘historical’ overview of this relative new field is presented. Basic governing mechanisms such as surface properties are discussed and, finally, the applications of wafer bonding are reviewed.

2.1. What is wafer bonding?

If two solids with clean and flat surfaces are brought into close proximity at room temperature, attractive forces pulls the two bodies together into intimate contact so that bonds can form across the interface. The first systematic investigation of this phenomenon was done by Lord Rayleigh [1], who performed interface energy and interface separation measurements on room temperature bonded, optically polished glass plates. These are the fundamentals of the emerging technology termed ‘Wafer Direct Bonding’, or ‘Fusion Bonding’. The phenomenon was given rather little attention until in the last decades when wafer bonding found several applications in mircomechanics, microelectronics and optoelectronics. The research and interest in wafer bonding, and especially semiconductor wafer bonding, has virtually exploded in the last years.

There are many factors governing the bonding behaviour of two surfaces. First of all, the surfaces must be flat and smooth. Usually it is argued that surfaces can make contact only at some asperities. However, the success of wafer bonding has followed the development of modern semiconductor chemo-mechanical polishing (CMP) technology. The semiconductor polishing technology has reached such a level of maturity that, nowadays, commercial silicon wafers have surface roughness in the order of Ångström. The second parameter governing the ‘bondability’ is surface chemical state and surface termination. For most semiconductors, surface preparation and cleaning techniques are well-developed and characterised. However, in silicon technology the surface chemical treatments are more standardised and established processes, as compared to for example compound semiconductors.

Terminology

This thesis contains research in ‘Direct Wafer Bonding’, or ‘Fusion Bonding’ which refers to bonding of wafers without any intermediate layer or adhesive layer at the interface, and is performed without applying an external electrical field. The basic procedure in semiconductor wafer bonding starts with ‘mirror polished’ surfaces that are cleaned, ‘activated’ and given their final surface termination using a combination of chemical treatments. The wafers are then brought together at room temperature,

and if proper surface conditions apply, the wafers will bond spontaneous. After room temperature bonding a heat treatment at elevated temperature is performed to strengthen the interface bonding. Typical wafer bonding procedures are fully compatible with microelectronic process technologies, offering several advantages both in available processing equipment and possible applications.

In the related field ‘Anodic Bonding’, sodium containing glass plates, mostly Pyrex, are bonded to silicon wafers under an applied external electrical field of 500-1000 V at elevated temperatures around 400 °C. Nearly all the applied field appears over a short depleted transition region in the glass close to the interface. Under the applied field mobile sodium ions in the glass migrate toward the cathode and oxygen ions migrate to the silicon anode where they react with the silicon wafer, forming a strong bond between the wafers. Anodic bonding is restrained to bonding of sodium containing glass plates with similar thermal expansion as silicon. However, anodic bonding is less sensitive to surface roughness as compared to wafer bonding and is an established technology in packaging and encapsulation of micromechanical sensors and actuators [2].

Other bonding technologies includes ‘Adhesive Bonding’ or ‘Eutetic Bonding’, where intermediate layers of polymers [3], spin-on-glasses [4] and metals [5] are used. Gold eutectic bonding is widely used in industrial device packaging. A silicon die is positioned on a gold layer that is plated on the package substrate. Applying a contact force and ultrasound to destroy the native oxide and increasing the temperature to the gold-silicon eutectic point result in the formation of eutectic compound at the interface. However, as mentioned above this thesis concerns ‘Direct Wafer Bonding’ and a short chronological approach to the development of wafer bonding will be given below.

A short ‘historical’ description

Widespread interest in modern wafer bonding techniques started in 1985-1986 when a research group from Toshiba presented silicon to silicon direct wafer bonding to serve as a substitute process for thick epitaxial layer growth of single crystalline silicon on silicon for potential application in power devices [6]. At the same time IBM presented direct bonding of silicon wafers with a thermally grown, electrically insulating, silicon dioxide layer. One wafer was thinned to a few microns to realise the first wafer bonded silicon-on-insulator (SOI) material [7]. Shortly after the microelectronic related work done at IBM and Toshiba, pioneering work in wafer bonding was done for application in micromechanics by Tenerz and Hök at Uppsala University [8]. Cavities and holes were realised using pre-structured silicon wafer for bonding. In 1988 Petersen and Barth presented a pressure sensor, using sealed

cavities fabricated by direct wafer bonding, which even went all the way to production [9]. They introduced the term ‘Fusion bonding’.

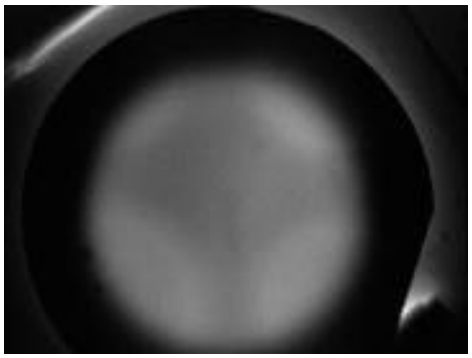

Figure 1. IR-transmission image of hydrophobic silicon wafer bonding after annealing at 1050 °C.

One of the great potentials of wafer bonding is the integration of dissimilar materials. Integration of dissimilar semiconductor by heteroepitaxial growth is hampered by the difference in lattice constants. Particularly, combining III-V compounds semiconductors with highly developed silicon circuits has been pursued in recent years with the goal to incorporate photonic and high-speed devices with advanced silicon technology [10, 11].

The epitaxial-layer transferring concept was presented as early as 1974 by Antypas and Edgecumb that bonded GaAs/AlGaAs epitaxial layers to a Corning glass substrate for fabrication of transmission photocathodes [12]. In 1989 Lehmann and co-workers were the first to achieve wafer bonding of InP and GaAs to Silicon. However, the annealing had to be kept below 160 °C to prevent the wafers from cracking and separating due to the thermal mismatch [13]. These works together with the work done by Liu and Mull [14] is seen as the inception of wafer bonding of III-V compound semiconductors.

2.2. Phenomenology of wafer bonding

The forces involved in room temperature wafer bonding are mainly short-range intermolecular and interatomic forces, such as van der Waals, capillary and electrostatic forces. Therefore, wafer bonding puts high demands on surface microroughness, cleaning and chemistry.

Surface roughness

Surface flatness, Total Thickness Variation (TTV), is a macroscopic measure, defined as the thickness deviation of the front surface of a wafer from a specified reference plane while the back surface is ideally flat. Periodic variation in surface flatness is sometimes termed ‘waviness’. Flatness in commercial semiconductor wafer is usually in µm range and therefore pose no obstacle in semiconductor wafer bonding, since flatness variations up to tens of µm can easily be accommodated through elastic deformation of the wafers during room temperature mating. The accommodation of the local flatness variation, waviness, can however induce a periodic strain pattern in the room temperature bonded wafers, which remains also after annealing at 1200 °C [15].

More important is the surface roughness. Gui and co-workers introduced the surface adhesion parameter

$$\theta = \frac{4E}{3(1-\nu^2)w}\sqrt{\frac{\sigma^3}{R}} \qquad (1)$$

to link the bondability of a surface to the surface microroughness [16]. E is Young’s modulus, ν is Poisson’s ratio, w is the surface enrgy and the surface roughness is described by spherical asperities having a radius R and a Gaussian height distribution with standard deviation σ. The bonding regime is defined by $\theta<1$ and the nonbonding regimes occurs when $\theta>12$. A decrease in surface roughness means the ‘real’ contact area increase and hence result in an increased bonding energy at room temperature. Development of industrial chemo-mechanical polishing (CMP) has efficiently improved the surface roughness of semiconductors. Advanced CMP technology achieves roughness (rms) in the Ångström range on commercial silicon wafers, and hence is not a hinder for wafer bonding applications. Even if tremendous developments has been achieve in CMP technology of other semiconductors, such as III-V compounds, the polishing technique has not yet reach the same level of maturity as in the advanced silicon technology. The final microroughness, of course, depends on subsequent surface process, such as cleaning, etching, film deposition, etc. For example, PECVD deposition or KOH etching of silicon or H_2SO_4:H_2O_2 surface cleaning of InP results in increased surface roughness. Figure 2 shows an AFM image of a PECVD deposited dielectric Bragg mirror on silicon. Due to the rough surface the attempt to bond SiO_2/Si_3N_4 dielectric Bragg mirror to an InP/InGaAsP active layer (1,55 µm) for the fabrication of an optoelectronic device unsuccessful.

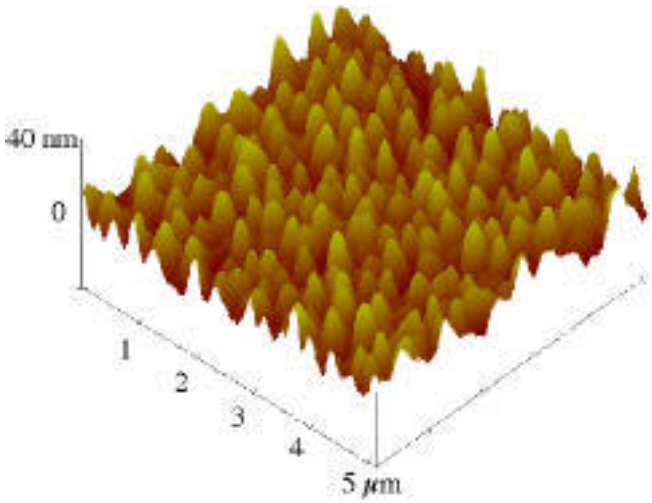

Figure 2. AFM image of the PECVD deposited SiO_2/Si_3N_4 Bragg mirror. The bonding to the InP/InGaAsP active region failed due to surface roughness (rms 6.07 nm).

Surface chemistry

'Traditionally' surface pre-treatments in wafer bonding are classified in hydrophobic or hydrophilic treatments. Usually hydrophilic semiconductor surfaces are covered with native or thermal oxides. The surface oxide is terminated by polar hydroxyl groups, OH^-, and therefore attracts polar water molecules. The water molecules present on the surface assist in spreading the 'bonding wave' and to form bridging between the mating surfaces during room temperature bonding. Upon the subsequent heat treatment the interface water either reacts with the surrounding oxide or diffuses away from the interface, so that covalent bonding is formed between the surfaces. At room temperature the linkage between surfaces in hydrophilic wafer bonding is achieved by two to three monolayers of water. Hydrophilic wafer bonding is therefore less sensitive to microroughness as compared to hydrophobic bonding.

Hydrophobic semiconductor surfaces are obtained by removing the native oxides in e.g. HF-solutions (GaAs native oxides can also be preferably removed in HCl or NH_4OH-solutions). When bonding hydrophobic surfaces there will be no mono-layers of water molecules present to assist the initial spreading of the 'bonding wave' and to form the initial bridging between the contacted surfaces. Instead a less polar, hydrogen terminated (with small amount of fluorine) surface is obtained. The exact mechanism for room temperature hydrophobic bonding is not fully understood, but weak van der Waals bridging between hydrogen terminated surfaces

or hydrogen bonds between fluorine and hydrogen is suspected to play a major role in hydrophobic room temperature bonding [17,18]. Therefore, hydrophobic bonding is more sensitive to microroughness. However, since no intermediate native oxide is present between the bonded wafers a crystal to crystal bonding will form when hydrogen is desorbed from the surfaces, during the following annealing step. This is in contrast to hydrophilic wafer bonding where, after annealing, the interface is composed of an amorphous intermediate oxide layer.

Contamination

A problem that sometimes occurs in wafer bonding is the presence of interface bubbles or voids. Macroscopic voids appear at the bonded interface due to i) trapped particles or dust contamination, ii) surface protrusion and iii) trapped gas. To avoid contamination of particles and dust on the surface before bonding, wafer bonding is preferably performed in a clean-room environment, or in a micro clean-room set-up [19]. Particles inhibit interaction between the opposing surfaces, and as a consequence a 1 μm dust particle trapped at the interface commonly results in an unbonded area (void) of 1 cm in diameter.

Gas bubbles occurs either by air trapping during room temperature bonding or more commonly during the subsequent heat treatment. The reason for formation of interface bubbles and voids upon storing or annealing is generally accepted as being nucleated by adsorbed hydrocarbons and increased in size by hydrogen entrapment [20]. Hydrogen is present both in hydrophobic and hydrophilic bonded interfaces (in hydrophilic bonding the hydrogen mainly originates from interface molecular water). In hydrophobic bonding, hydrogen is generated from surface hydrides during annealing:

$$\equiv Si - H + H - Si \equiv \Rightarrow \equiv Si - Si \equiv + H_2 \qquad (2)$$

In case of hydrophilic bonding, hydrogen is created from reaction with interface water molecules:

$$Si + H_2O \Rightarrow SiO_2 + 2H_2 \qquad (3)$$

Hydrogen diffuses along the interface until they nucleate at locations of hydrocarbons or other interface cavities. When the pressure from trapped hydrogen gas exceeds the energy of adhesion a macroscopic void is formed. In silicon wafer bonding voids typically appear when annealing in the temperature range 200-800 °C. Annealing above 800 °C usually makes the gas-filled voids disappear completely. Special care has to be taken in choosing proper surface treatment in order to avoid void formation. Other techniques to avoid formation of voids

includes: bonding the wafers under vacuum condition, pre-etching wafers to make arrays of channels at the interface for the escape of trapped gases, pre-heating the wafers at 600-800 °C in argon or oxygen ambient, to oxidise and desorb hydrocarbons before bonding.

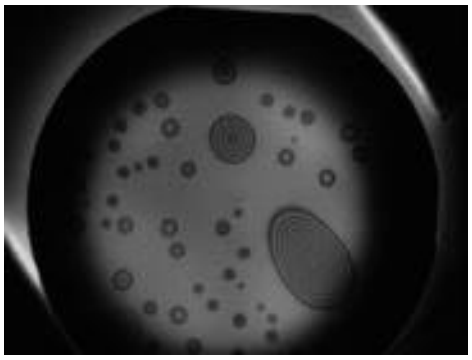

Figure 3. IR-transmission image of hydrophobic silicon wafer bonding after annealing at 700 °C. A lot of interference patterns are seen, caused by interface bubbles.

Ionic contamination represents another category of contaminants. These contaminants mainly affect the electrical properties of the bonded interface. Especially boron from the clean-room environment has been proposed as a serve contamination in wafer bonding. Boron contamination of the surfaces before bonding results in a p-doped layer near the bonded interface after annealing [21].

Thermal treatment

When the wafers have been bonded together at room temperature usually the interaction, or bonding energy, is relatively weak. Therefore, a heat treatment is performed to increase the bond-strength. The annealing enhances out-diffusion of interface trapped molecules and desorption of chemisorbed surface atoms, such as hydrogen. At the same time the annealing activates formation of covalent bonds between the bonded surface, like crystal-to-crystal bonding in the case of hydrophobic bonding. A detailed review on the mechanisms involved in silicon bonding upon annealing is found in [22]. In wafer bonding involving III-V compounds an interface mechanism of atomic rearrangement has been reported [23]. The thermal treatment used to increase the bond-strength can, unfortunately, also cause severe problems in wafer bonding. For instance, when bonding dissimilar materials the thermal mismatch induced high stresses in the material. This will discussed in more detail in Section 4.2. High temperature annealing also restricts the use of metal patterns and can cause diffusion of dopants.

2.3. Applications

The main driving force for development of direct wafer bonding has indisputably been the realisation of SOI material with device layer having bulk silicon quality. But over the years wafer bonding has been established as routine process also for MEMS applications. In the area of compound semiconductors the commercially most important application of wafer bonding is the visible AlInGaP light-emitting diodes (LEDs) introduced by Hewlett Packard. Using wafer bonding the absorbing GaAs is replaced by a transparent GaP substrate and a twofold improvement of luminous efficiency is achieved [24].
However, there is a rapid development in wafer bonding and a number of high potential applications are emerging.

Silicon-on-Insulator (SOI)

In most electronic devices only a small fraction of the total wafer thickness is used for electron or hole transport. Isolating the thin device layer electrically from a support wafer or handle wafer offers several advantages. Initially, radiation hardness in military space application was the prime target for realising SOI material. With time the main purpose of using SOI materials has somewhat changed. The electrical isolated device layer in SOI improves device performance in two fundamental ways: first it reduces the operating volume of silicon that need to be charged to switch the transistor on and off, and secondly it isolates the transistor from its neighbouring transistors and other circuit components with a layer of insulator material (silicon dioxide). In SOI CMOS technology one distinguish between fully depleted or partially depleted devices. In fully depleted devices the depletion region extends throughout the device-layer. The front-run technologies to produce SOI wafers are separation-by-implantation-of-oxygen (SIMOX) and direct wafer bonding approach. A comparison between these two techniques is found in [25]. In the wafer bonding approach two oxidised Si wafer are bonded together, creating the buried oxide, one of the bonded wafers is then thinned to a desirable thickness, which constitutes the devices layer. The SOI fabrication techniques utilising wafer bonding, mainly differs in thinning procedures. Traditionally bond-and-etch-back (BESOI) technologies has been used but in recent years layer-splitting technologies has emerged in being more competitive, first because of excellent control of device-layer thickness and secondly because the Si substrate from which device-layer is split can be re-used. One of these splitting technologies is named ‘Smart-Cut’ [26].

The Smart-Cut process flow is schematically shown in Fig. 4. Before bonding hydrogen ions are implanted in one of the wafers. The wafers are then bonded and heated, which leads to the development and growth of hydrogen induced

microcracks parallel to the bonded interface. The growth of the microcracks proceeds until complete splitting occurs. After splitting the bonded wafers are further annealed to increase the bonding strength. Finally, the surfaces are slightly polished, the SOI material is ready and the wafers from which the device layer was split can be re-used for subsequent splitting. Layer-splitting of materials including GaAs, InP, diamond and SiC has also been demonstrated and different implantation ions have been used [27, 28].

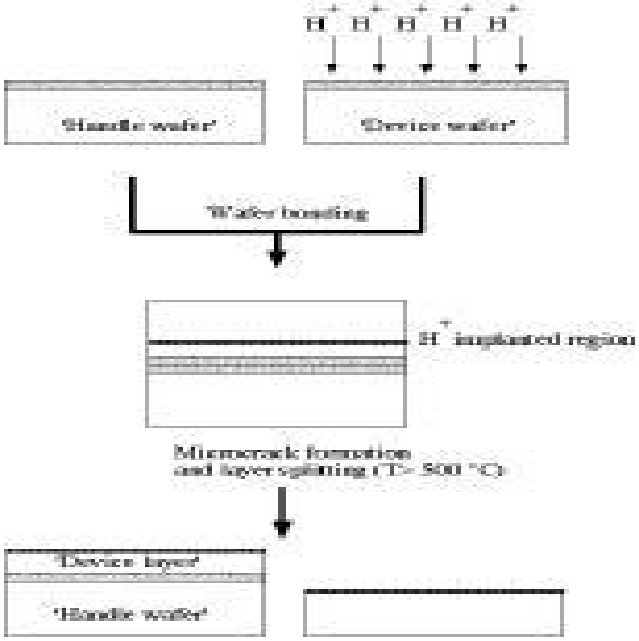

Figure 4. Principle of the Smart-Cut process.

Other wafer bonding and layer transferring techniques for SOI are Eltran [25] and the Genesis Process [29].

Micro Electro Mechanical Systems (MEMS)

Several high-volume MEMS devices have been realised using wafer bonding. A comprehensive review of commercial MEMS devices and a future outlook of wafer bonding as a tool in high-volume MEMS products is found in [30]. Wafer bonding allows assembling of pre-structured wafer into ready sensors. Cavities and holes used in many pressure sensors, automotive sensors are realised using wafer bonding.

Dissimilar materials integration

The freedom to integrate diverse materials is one of the advantageous features of wafer bonding. In design no consideration has to be taken to use lattice-matched materials. Several high-potential applications are reported using dissimilar materials

integration by wafer bonding. As mentioned above Hewlett-Packard already have a commercial success with wafer bonded AlInGaP LED. Levine et al. have demonstrated a ultralow-dark-current 20 GHz photodetector using an InGaAs absorption layer and a Si avalanche multiplication layer [31]. Others have solved the problem of poor quality InGaAsP/InP mirrors in vertical-cavity surface emitting lasers (VCSELs) by wafer fusing high-reflecting GaAs/AlGaAs mirrors to the InP-based long-wavelength (1.3μm or 1.55μm) active region, e.g. [32]. Fabrication of GaAs and InP-based lasers directly on Si substrates have also been achieved using wafer bonding [33].

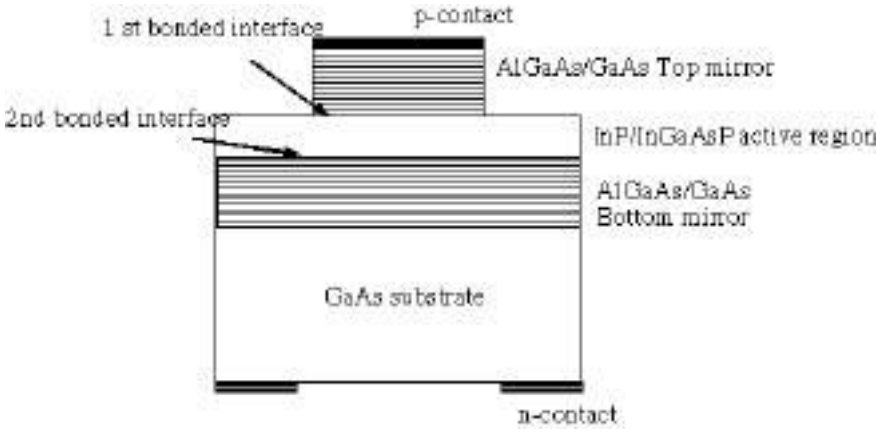

Figure 5. Wafer fused long-wavelength VCSEL.

Bonding of ceramics films (e.g. $Bi_4Ti_3O_{12}$) to dissimilar substrates has also been reported [34], which avoids undesirable diffusion between the ceramics and the semiconductor substrate that occurs during high-temperature deposition. A review of dissimilar material integration using wafer bonding is found in [35].

Another interesting and widely argued application of wafer bonding is the fabrication of fixed film compliant substrates [36]. Ideally, compliant substrates are composed of a free-standing thin film, which during subsequent heteroepitaxial growth will deform elastically to accommodate the lattice mismatch between the growing film and the 'substrate', else the elastic strain would be relaxed by generation of misfit dislocation. This hence allows growth of dislocation-free hetero-epitaxial films beyond the Matthews-Blakeslee critical thickness. It has been shown that compliant substrates may be achieved also by wafer bonding a thin film that is intentionally bonded with a twist angle relative to the substrate. During subsequent heteroepitaxial grown this twist wafer bonded thin film accommodates the elastic strain in the growing film. However the actual affect of the twist bonded thin film is still an issue of debate. Free-hanging thin films are not suited for industrial application but by twist wafer bonding fixed thin films compliant

substrates can be realised. A fixed film compliant substrate is more suited for device fabrication after heteroepitaxial growth.

3. CHARACTERISATION AND PROPERTIES OF WAFER BONDED STRUCTURES

In this Section characterisation techniques that have been used in this work are presented. The techniques are outlined briefly and then a short description on how they were applied and what was investigated using these techniques. Some characterisation methods that have been developed within this work are portrayed more in detail, such as surface energy measurements and defect-etching techniques.

When working in wafer bonding there is a need both for pre-bonding analysis and post-bonding evaluation. Pre-bonding analysis generally involves roughness measurement or chemical analysis in order to investigate the surface 'bondability', but it can also consist of evaluating device layers before bonding. Post-bonding characterisation is more focused on evaluating the mechanical, electrical or optical properties of the wafer bonded junction and the wafer bonded material.

3.1. Surface characterisation

Roughness

Smooth surfaces are crucial in wafer bonding. A rough estimation is that a hydrophilic silicon surface has to have a rms value below 0.5 nm to bond spontaneous. When analysing surface roughness of this order of magnitude the most direct approach is to use scanning probe microscopy (SPM) techniques. In this work contact mode atomic force microscopy (AFM) was vastly used. In contact mode AFM the surface is scanned with a probe (a cantilever with a very small tip) and the deflection of the either cantilever or more frequently the sample stage is monitored to retract a picture of the surface. AFM is fast, direct and easy to use, it put no constrains on samples and do not require vacuum environment. The height resolution is in the order of 0.1 Å and it has an excellent lateral resolution of about 10 Å. AFM was mainly used to investigate the roughness (smoothness) resulting from surface cleaning and preparation procedures carried out before bonding. However, AFM was also used on wafers that debonded, to trace the cause of bonding failure, e.g. caused by a too rough surface or the creation of surface protrusion during annealing etc.

Surface chemistry

XPS—X-ray photoelectron spectroscopy (XPS) has been developed to a very useful tool to investigate surfaces and near surface chemistry. XPS gives information about elements present of the surface and information about the chemical states of these

elements. The sample to analyse is irradiated by photons having a determined energy hν (monochromatic X-ray). Through the photoelectric effect the sample then emits electrons (photoelectrons). From the energy spectrum of the emitted photoelectrons information about the bonding energy of the atoms present on the surface is obtained.

$$E_{kin} = h\nu - E_B \quad (4)$$

E_{kin} is the kinetic energy of the emitted photoelectrons, E_B is the binding energy. Since each element is characterised by a specific composition of ionisation energies (bonding energies), the elements can be traced from the emitted energy spectra.
XPS is especially advantageous for surfaces and near surface analysis since the signal (emitted electron) comes from a very thin near-surface layer (approximately 10-20 Å). For good signal and detection of an element it has to compose approximately 1% of an atomic layer (all elements except hydrogen can be detected). The concentration of elements is obtained by measuring the intensity at each element peak in the energy spectrum. Similar element information from a surface can be obtained using Auger Electron Spectroscopy (AES), however the main advantages of using XPS is that information about the surroundings of an element can be obtained through the chemical shifts. XPS, or ESCA (Electron Spectroscopy for Chemical Analysis), was originally developed at Uppsala University by K. Siegbahn [37].
In this work XPS was often used to track native oxides, to see whether it was removed or not after e.g. surface treatment in HF solutions and to determine if the bonding mechanism was hydrophilic or hydrophobic [Paper IV, V]. XPS was also utilised to estimate and compare the composition of native oxides after surface pre-treatments. For instance, oxygen plasma exposure of InP surface resulted in a thin surface oxide of very different composition and thickness compared to surface treatments in oxidising wet-chemical solution. It was concluded that phosphorus had been ‘lost’ during oxygen plasma exposure and this was believed to affect e.g. the C-V characteristics of wafer bonded InP MOS structures [Paper VI].

Ellipsometry—When an electromagnetic wave encounters a material, it is transmitted, absorbed and/or reflected. The modification of the reflected light relative to the incident light is governed by optical properties of the material. Therefore, the reflected light contains a lot of information about the irradiated matter.
The basic idea in ellipsometry is to measure the ellipsometric parameters Δ and Ψ. Δ is defined as

$$\Delta = \delta_1 - \delta_2 \quad (5)$$

δ_1 is the phase difference between perpendicular components of the incoming electromagnetic wave and δ_2 is the phase difference between perpendicular

components of the reflected electromagnetic wave. Δ is therefore the change in phase between the perpendicular component of the electromagnetic wave that occurs upon reflection. Without regard to phase, the amplitude of perpendicular components of the electromagnetic wave may change upon reflection. Ψ is defined as

$$\tan \Psi = \frac{\left|R^p\right|}{\left|R^s\right|} \qquad (6)$$

R^p is the amplitude ratio, before and after reflection, of the electromagnetic wave component parallel to plane of incidence. R^s is the amplitude ratio of electromagnetic wave component perpendicular to plane of incidence before and after reflection. Starting from these parameters different models are applied to calculate refractive indices, film thickness, etc. The correctness of the results depends very much on the correctness of the applied model.

The basic components of an ellipsometer system are the laser that generates monochromatic unpolarised light, a polarizer to create linearly polarised light, the Quarter-wave plate (QWP), an analyser and a detector. Historically the QWP was placed in the light-path after the reflection from the surface (the linear polarized light is converted to ellipically polarized light by the surface reflection and the QWP converts the elliptically polarized light back to linear polarization so that the analyser and the detector can determine the 'null' or polarisation of the reflected light) but in common practice the QWP is positioned before surface reflection. One of the reasons for using this configuration is that the relationship between the settings of the polarizer and the analyzer and the values of Δ and Ψ is simpler, e.g. [38]

Ellipsometry was utilised to determine the thickness of thin oxides grown on Si and InP-based materials after oxygen plasma treatment. For Si this is a commonly applied technique, but for the InP-based material (InGaAs, InGaAsP, etc) the technology is more immature so only rough estimation could be made from spectroscopic ellipsometry. Ellipsometry was also used to measure the plasma induced damages (bombarding ions in the plasma creates a damaged surface-layer). The method was developed by J. L. Beckner et al. [39], and basically consists of the modelling the silicon surface with a simple two-layer model consisting of a silicon dioxide top layer and beneath a damaged silicon layer, Fig. 6.

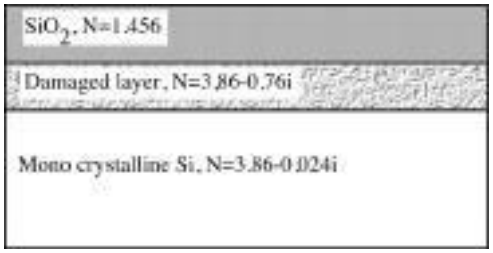

Figure 6. Ellipsometric model used to study surface properties after oxygen plasma treatment.

Most of the basic equations in ellipsometry use the assumption of plane parallel interfaces; surface roughness has therefore to be modelled separately. Since the oxygen plasma gives very smooth surface this is a fairly good approximation. However, for surface treatments that resulting in increased microroughness care has to be taken. This was seen to be the case for RCA-1 treated Si surfaces, since the results on oxide thickness deviated from what could be expected [Paper II].

3.2. Structural and mechanical properties

Structural properties

Crystal defects—if two identical crystals with the same orientation are bonded together without misalignment and without interface contamination, the two crystals should merge into one. However, in real life there are always deviations from the ideal case. In wafer bonding there is always an inevitable misalignment between the bonded wafers and therefore misfit dislocations appear. Misfit dislocations will also appear at the bonded interface if two crystals of different orientation or different lattices are bonded. The presence of native oxides, adsorbed surface contaminants and interface bubbles (voids), also inhibit a perfect crystal-to-crystal transition region. In silicon wafer bonding the increase or decrease of the interfacial oxide is linked to proper alignment and to the oxygen content in the silicon wafers. The interface oxide has shown to increase when bonding Czochralski (CZ) Si wafer and respectively decrease when bonding high purity Float Zone (FZ) Si wafers [40]. In wafer bonding involving III-V semiconductors an atomic re-arrangement of the interface has been observed. Atomic diffusion of indium or gallium, which is activated at elevated annealing temperatures, fills up interface irregularities that are present at the bonded junction [41]. Many of the detailed interface investigation are carried out using transmission electron microscopy (TEM), see e.g. [42-44].

In this work defect-etching techniques were found to be more suited for investigations of bulk material defect introduced by wafer bonding, arising mainly from thermal mismatch stress. Defect-etching uses etch selectivity to reveal crystal imperfection such as dislocation. The dislocation appears as pits and from the shape of the pits its origin is traced, be it point or volume defects. A detailed correlation of etch pit shape and material defects in InP is found in the work by A. Knauer et al [45]. If TEM analysis is very useful in fundamental studies, defect-etching is easier, quicker and a more direct approach. It allows investigations of large areas and in combination with chemical thinning it was possible to map the dislocation density throughout a whole wafer. For Si and III-V semiconductors defect-etching techniques are well developed and frequently used, by e.g. wafer manufacturer. Examples of Si defect-etchant are Dash, Secco and Wright [46] and the most

frequently used defect-etchants in InP (to reveal dislocations) are Huber-etchant and A/B etchant [47,48].
Other techniques that may be used to investigate crystal defects and stress are photoluminescence (PL) and X-ray diffraction (XRD).

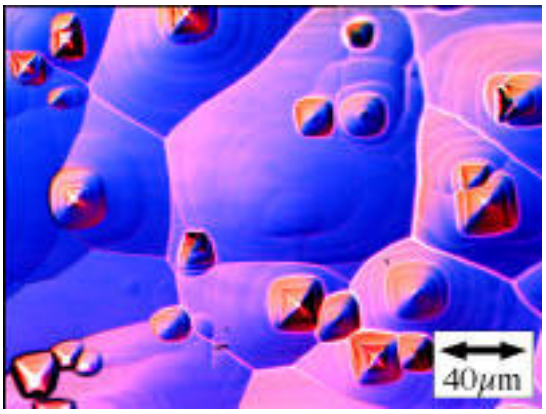

Figure 7. Defects in InP-to-Si wafer bonding. The dislocations created in InP due to thermal mismatch stress during annealing are revealed using Huber etching.

Detection of voids—There are several techniques available to detect interface bubbles or voids at the bonded interface. The easiest and most frequently used is infrared (IR) transmission imaging. The bonded wafer pair is irradiated with light from a tungsten lamp and the transmission is detected using an IR sensitive camera. Undulations at the interface such as voids will appear as interference patterns (Newton rings). IR transmission imaging is very fast and allows the bonding to be examined while being performed. The light source, the band-gap of bonded materials (light absorption yields that $\lambda > E_g$) and the detection limit of the IR-camera determine the resolution of the technique. In a standard IR camera set-up for Si wafer bonding inspection the height resolution is about 250 nm.

Figure 8. IR-camera inspection set-up.

The height resolution can be improved using X-ray Topography (XRT) and even smaller microvoids can be observed by TEM investigations of the interface. These techniques are however much more complicated and time consuming.

Bond-strength evaluation

An important parameter to characterise in wafer bonding is the adhesion between wafers. Most frequently the surface energy is used as a measure of the adhesion. The surface energy is linked to the energy required to separate the wafers. Surface energy measurements are generally carried out using the crack-opening method, which is a fast and easy technique. By inserting a thin metal-blade in-between the bonded wafers and measuring the resulting crack length, using IR-transmission, a value of the surface energy γ is obtained from

$$\gamma = \frac{3Et^3y^2}{8L^4} \qquad (7)$$

where E is Young's modulus, t is the wafer thickness, 2y is blade thickness, and L is the measured crack length [49]. However using the crack-opening method errors are easily introduced since (i) the method depends on how the blade is inserted (a process often done manually), and (ii) because the measured surface energy is dependent on the measurement conditions. As a consequence there are large variations between results obtained by different research groups. To obtain more reproducible and absolute values, an alternative way of measuring the surface

energy at room temperature was proposed [Paper III]. The method consists of introducing controlled spacers in the bond-interface and measuring the resulting non-bonded area. These spacers are called ‘mesa-spacers’ since lithographically defined silicon dioxide mesas were used as spacers. During mating of the wafers the spacers will inhibit the bonding in its surroundings, the extension of the unbonded area is determined by the surface energy. Another advantage of using the ‘mesa-spacers’ method to measure the surface energy is that it allows a nondestructive and noncontaminating way of measuring the surface energy. Therefore, the bonded wafers can be further processed, whereas using the crack-opening method damage and contamination may be introduced.
Another common technique to measure the bond-strength is tensile-testing which has the advantage of being able to measure very high bonding-strength, when blade insertion is not possible [50].

3.3. Electrical properties

The electrical properties of wafer bonded interface has been investigated by several groups, both for hydrophilic and hydrophobic wafer bonding and also for wafer bonding involving compound semiconductors. A generalised theory for wafer bonding may be difficult to achieve since the electrical properties of the wafer bonded interface depends on a number of parameters. The electrical properties vary between different reports and it is likely that such deviations are linked to variations in bonding procedures. Hydrophobic interface of course leads to lower junction resistance compared to hydrophilic interface, since the native oxide has been removed. Also, care has to be taken in properly removing contaminants, metallic and organic, from the surfaces before bonding. The disordered interface being composed of misfit dislocation acts as gettering and segregation site in the same way as grain boundaries in polycrystalline semiconductors. Misalignment between the crystals has been reported to increase junction resistance due to electrical charging of misfit dislocation. When bonding compound semiconductors, crystallographic aligning of the bonded wafers to an angle below 4 ° reduced the junction resistance, irrespectively of the lattice mismatch between the wafers [51].

A model based on thermionic emission over a potential barrier resulting from charged interface states was presented by S. Bengtsson, e.g. [52], for unipolar wafer bonded junctions. Assuming that the electron can tunnel through the interface oxide in hydrophilic bonding, the increased junction resistance was described by the interface charge trapping. The interface charge trapping increase with applied bias, which counteracts the decrease of the potential barrier and hence accounts for the slow increase of current with applied bias. Using hydrophobic bonding the charge trapping at the interface is heavily reduced in unipolar structures. Other models

states that the amorphous interlayer in hydrophilic bonding acts as a tunneling barrier for charges [53].

Wafer bonded p-n junction characteristics are heavily affected by the non-ideal interface. However, a substantial improvement of wafer bonded p-n junctions characteristics is usually obtained by shifting the p-n transition away from the bonded interface, either by high temperature annealing (1200 °C) [54] or by implantation [55,56]. Alternatively p-n junction wafer bonded under UHV conditions and low temperatures resulted in an ideality factor of 1.18, indicating low recombination at the interface. Wafer bonding Si p-n junction in ambient air and subsequent high temperature annealing was seen to yield high recombination near the bonded interface. An ideality factor of 2 was obtained and low minority carrier lifetime. The generated electrical defects increased in wafer bonded junctions annealed at 1050 °C compared to compared to samples annealed 700 °C [paper VIII]. Figure 9 shows the I-V characteristics of wafer bonded Si p-n junction annealed at 700 °C and 1050 °C. Most often the bonded interface is avoided in the electrically active region of electronic device. However, the recombination centres of the defective wafer bonded interface has been used to control the minority carrier lifetime in power devices. The bonded interface was introduced in the lightly doped p-base region to reduced minority carrier lifetime, which was beneficial for switching time control [57].

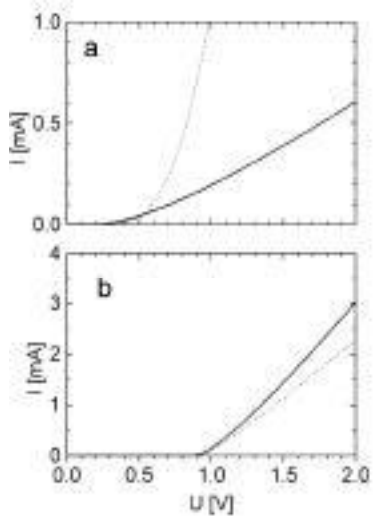

Figure 9. I-V characteristics in dark measured at 300 K (a) and at 100 K (b) of wafer bonded p-n junctions annealed at 700 °C (dotted lines) and 1050 °C (full lines).

4. LOW TEMPERATURE SEMICONDUCTOR WAFER BONDING

Generally, wafer bonding requires a high-temperature annealing step to ensure the formation of strong bonding between wafers, i.e. to form covalent bonds. In silicon-to-silicon wafer bonding usually an annealing above 1000 °C is required, and in wafer bonding involving III-V semiconductor compounds the annealing is usually performed above 600 °C. Such a high-temperature annealing is incompatible with many application. Particularly, pre-structured wafers that already contain temperature-sensitive structures cannot be exposed to the high-temperature annealing. The high-temperature annealing also induce material degradation. It can cause broadening of diffusion layers, and annealing above 450 °C cause severe damage to aluminium patterns. Especially, when bonding dissimilar materials the high-temperature annealing induces large thermal stress due to the difference in thermal expansion. The thermal stress can be detrimental for the results, for instance it can make the bonded wafers crack as will be seen below.

Therefore, all the way back to the pioneering days a lot of the effort and research in wafer bonding is focused on developing low-temperature wafer bonding procedures. A number of techniques have been developed in order to reduce the annealing temperature in wafer bonding, e.g. [58-63].

In this work the use of plasma activation of the surfaces before bonding has been examined, in order to achieve a low-temperature wafer bonding procedure. To optimise the procedure, first the influence of the plasma parameters were investigated and a specially designed fixture was developed to enable *in situ* wafer bonding. Finally, oxygen plasma activation was applied to integrate InP-based materials with Si by direct wafer bonding. This material combination is highly interesting for the realisation of future optoelectronic integrated circuits (OEIC).

4.1. Plasma assisted wafer bonding (PAWB)

Plasma processing

Chemically reactive plasma discharges are widely used to modify the surface properties. The relative importance of a specific discharge depends on input power, gases, reactor volume and geometry, gas flows, etc. For instance, plasma discharges are employed for etching, deposition or surface cleaning. The gas-chemistry and the plasma parameters (effect, applied voltage, pressure, plasma density, etc.) that are being used govern the plasma/surface interactions. A variety of gases are at hand, e.g. O_2, SF_6, Ar, Cl_2, CHF_3 to name a few. Different techniques to generate discharges are available—dc, rf, magnetron and also a variety of plasma reactor

system are being used, e.g. reactive ion etching (RIE), inductively coupled plasma (ICP) or electron cyclotron resonance (ECR), but far from limited to those. A comprehensive review of plasma process technologies is found in the book by Vossen and Kern [64].

The plasma affects a surface mainly in two ways — physically and chemically. Physical plasma/surface interaction is due to bombardment of energetic ions. The bombarding ions cause sputtering, mixing and defect formation. Chemical interaction is driven by chemically active species in the plasma.

A plasma is a partially ionised gas with equal number of positive and negative charges. At steady state the free electrons acquire sufficient energy from the applied electric field to produce impact ionisation of the gas, at a rate equal to the loss rate. Since the electrons are more mobile (due to lower mass) they diffuse faster to the surrounding surfaces, including substrate surface and chamber wall. This builds up a negative potential at the surrounding surfaces, while the plasma is 'depleted' from negative charges. Therefore, the *plasma potential* is always positive. As a result, the electric field between the positively charged plasma and the negatively charged surroundings, induce an ion current, that is equal to the electron diffusion current at equilibrium. A body immersed into a plasma hence acquires a negative potential, *floating potential*. The ions in the plasma are accelerated through the plasma sheat and 'bombards' the surrounding surfaces. However, by applying an external field the energy of the ions bombarding the substrate can be adjusted. Many capacitive discharges are asymmetric, because the rf-driven electrode area is smaller than the grounded area (usually the chamber wall). This causes the driven electrode to acquire a dc offset, *self-bias voltage.*

Oxygen plasma is especially attractive for surface pre-treatment in wafer bonding since it is known to be very efficient in removing hydrocarbon and water related species.

Oxygen plasma assisted wafer bonding

For the oxygen plasma exposure a reactive ion etching (RIE) system was used. The system had been modified, a push-rod allowed both wafers to be processed simultaneously and to be bonded *in situ* the vacuum chamber without exposing them to ambient air after oxygen plasma treatment. Figure 10 shows the experimental set-up. The silicon wafers have been loaded in the RIE and are being exposed to an oxygen plasma. Immediately after oxygen plasma treatment the silicon wafers are brought in contact inside the RIE system using the push-rod.

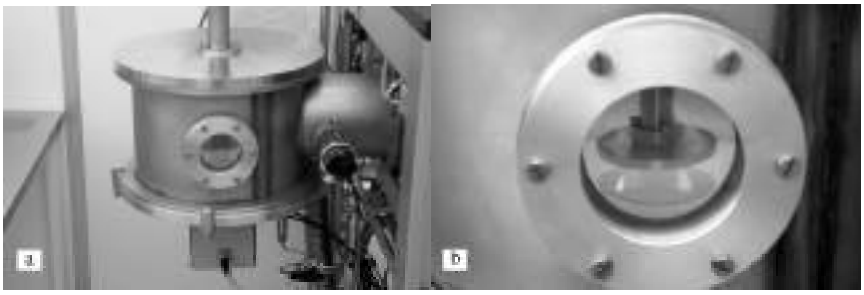

Figure 10. Experimental set-up for *in situ* plasma wafer bonding. In a) the complete apparatus is shown and b) shows a close-up view of the wafers during plasma exposure.

During the course of this work it was seen that the results of wafer bonding properties depended on the discharge parameters used. This is due to the fact that the surface conditions are governed by discharge conditions. Therefore, much effort was focused on optimising the plasma parameters for wafer bonding applications. Especially the self-bias voltage of the plasma was an interesting parameter to study, since it is related to the energy of the impinging oxygen ions. But also other plasma parameters were seen the have an impact on the results.

Silicon wafers were bonded together *in situ* after surface treatment in the oxygen plasma, with self-bias voltage ranging from 0V to –360 V at a pressure of 56 mTorr and a flow of 30 sccm. Surface energy measurements were performed on the bonded silicon wafers using the crack-opening method. It was seen that the surface energy of the bonded wafers depended on the discharge conditions. Figure 11 shows the surface energy as a function of self-bias voltage in silicon wafer bonding. The best results regarding both voids density and bond-strength were found when using oxygen plasmas having moderate self-bias voltage. For wafers bonded *in situ* under oxygen flow but in absence of a plasma (0V self-bias voltage), no substantial improvement was achieved compared to the reference measurement made on silicon wafers bonded in ambient air after standard RCA-1 treatment. It is also seen in Fig. 11 that the bond-strength was not increased when high self-bias voltages were applied, compared to the reference measurements [paper I and II].

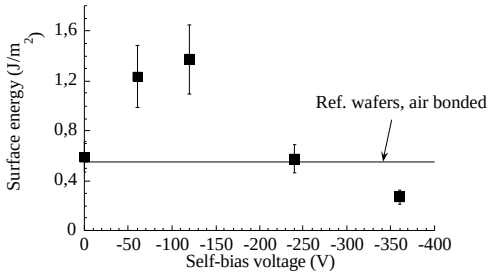

Figure 11. Surface energy in silicon wafer bonding as a function of self-bias voltage after annealing at 200 °C.

AFM images of the oxygen plasma treated silicon wafers revealed that the thin oxide grown by the oxygen plasma treatment is very smooth, which is beneficial for wafer bonding applications. However, the high bond-strength obtained after oxygen plasma exposure is not believed to be link solitarily to the smooth surface. The thin oxide grown by oxygen plasma exposure was seen to be very hydrophilic; the surface is more hydrophilic than after a standard RCA-1 treatment or other hydrophilic wet-chemical treatments. This could indicate that the oxidation generated by the oxygen plasma exposure have very strained Si-O-Si bonds, that hence are very reactive since they are more likely to brake and form new bonds [35]. Other authors have reported increased oxidation kinetics after oxygen plasma treatment as being responsible for the increase in bond-strength, the interface water is 'consumed' at a faster rate and at lower temperatures. This process is more efficient for *in situ* wafer bonding compared to *ex situ* wafer bonding [65].

Ultra-thin oxides (< 5 nm) grown by plasma oxidation are being extensively studied as a low temperature oxidation alternative for future ultra-large-scale integrated circuits (ULSI) [66]. The oxidation mechanism in plasma oxidation is different from that of thermal oxidation and although being subject of extensive research the exact mechanism of plasma oxidation is not yet fully understood. Active chemical and charged species in the presence of a potential profile in the growing oxide makes the growth mechanism very complicated [67]. However the presence of charged oxygen species have been indicated as being the main reason for the low temperature oxidation and many of the properties of the grown ultra thin oxides are governed by the energy of the impinging ions. In consistency with our result, Table 1, several authors have reported that an increase in the energy of the impinging oxygen ions (either positive or negative) yields a higher oxidation rate, e.g. [67]. The energy of the bombarding oxygen ions not only determines the oxidation rate but also influences several other properties such as stress, density, structure and electrical properties of the ultra-thin silicon dioxide films [68]. Therefore, the properties of thin silicon dioxide grown by oxygen plasma exposure varies at different self-bias voltages, which was also seen to have an impact on oxygen plasma activated wafer bonding.

Table 1. Ellipsometric parameters for various Si surface treatments.

Surface treatment	Δ	Ψ	Oxide thickness (nm)	Damaged layer (nm)
Native oxide	177.31	23.28	0.6	0
HF	177.99	23.28	0	0

Oxygen plasma(-120V)	176.89	23.41	1.1	0.5
Oxygen plasma(-360V)	174.01	23.51	4.0	1.0

Finally, low temperature fabrication of Si MOS (metal oxide semiconductor) structures was realised by transferring of thermally grown SiO_2 to Si wafer using oxygen plasma wafer bonding [paper VI]. It was shown that oxygen plasma wafer bonding might be an interesting alternative for low temperature fabrication of SOI material, but the procedure may need further optimisation.

Low temperature oxygen plasma wafer bonding procedures are interesting for a number of applications and currently several other groups are conducting research in this area [69,70,71]. Oxygen plasma assisted wafer bonding has also previously been presented by other authors [72,73]. Recently, oxygen plasma wafer bonding has been utilised in combination with room temperature controlled nano-cleaving tool to fabricate commercial SOI wafers. The process is termed Genesis Process™.

4.2. InP-to-Silicon direct wafer bonding

Integration of InP and Si has attracted much interest since the unique properties in each material can be combined in devices or systems, e.g. combining InP-based optocomponents with the well-developed microelectronic circuitery for intra or interchip optical interconnects.

The epitaxial growth of InP-based materials on Si substrate is hampered by the 8.1 % difference between the lattice constants of the materials. However, using wafer bonding for the integration the lattice-mismatch becomes no obstacle. Unfortunately, there is also a large difference in thermal expansion between InP and Si. When bonding wafers of dissimilar materials and annealing at elevated temperatures, the thermal mismatch will induce high thermal stress in the material.

In this Section the problems arising in InP-to-Si wafer bonding due to high-temperature annealing and thermal stress are described. Finally, low-temperature InP-to-Si wafer bonding and InP-based epitaxial layer transferring using oxygen plasma surface activation is presented.

Introduction

In each material system, nature has dictated a set of physical properties, such as mobility, optical absorption, resistivity, thermal and mechanical properties. For a given application the optimal properties may not reside in a single material but in a variety of disparate materials. A specific case is to combine III-V compounds that have direct bandgap and high mobility with Si that is extensively used in microelectronic applications.

For lattice-matched materials systems such as GaAs/AlGaAs or InP/InGaAsP the material integration is extensively and routinely realized using heteroepitaxy. However, for material systems that are largely lattice-mismatched, such as InP/Si (8,1% lattice-mismatch), heteroepitaxial growth has not been able to produce the high quality material needed in e.g. OEICs [74-76]. Heteroepitaxial growth of InP-based materials on Si has been a subject of keen interest and although improvement is continuing, the densities of threading dislocations in InP seem to have saturated at around $10^7 cm^{-2}$, more than ten thousand times higher than the value for lattice-matched epitaxy on InP. The dislocation density at the interface of heteroepitaxial grown InP/Si junctions is found to be around $10^{10} cm^{-2}$. The dislocation density and material quality have however been improved by 'indirect' growth of InP on Si using GaAs intermediate buffer layers (GaAs is 4% mismatched to Si and 4% mismatch to InP) or various epitaxial layer overgrowth (ELO) and conformal growth techniques. The principal feature in ELO is that growth proceeds laterally over a cap-layer, which block and inhibit transmission of threading dislocation.
The applications for integrating InP-based material with Si can be divided into three categories, were each category has its own constrain on interface and material properties.

I: The unique properties of each material are combined in devices to reach optimal performance: e.g. an avalanche photodetector has two functions absorption of light and conversion of light into an electrical signal. Therefore InGaAs epitaxial layers were bonded to Si substrate, the InGaAs has high light absorption at 1,3 µm and 1,55 µm while Si has a much higher electron/hole ionisation ration leading to higher avalanche multiplication efficiency [55].

II: Integration of InP-based optoelectronic and high-speed devices with Si microelectronic circuits: Optical interconnections are very desirable since they can overcome the electrical interconnect bandwidth bottleneck. Optical communication links finds application in both rack-to-rack, board-to-board and intra and interchip connections [77]. The integration of InP-based optoelectronics with Si VLSI circuits may be especially advantageous since Si is transparent at 1,3 µm and 1,55 µm. Therefore optical communication can take place within Si bulk, which facilitates back-surface integration of micro-optics (beam reflectors, DOE). The most straightforward approach, flip-chip bonding, which is currently used to form hybrid OEICs, suffers from an inherent throughput limit when multiple optical nodes exist in each die. Further more, thermal stress, solder under-filling, and non-planar surface profiles present additional difficulties for vertical integrated optoelectronics.

III: Si as substrate for InP; Relieving the strain from InP substrate industry. The boom in compound semiconductor industry has implied the need for larger-diameter wafers. At present this is much more evident in electronic applications than in optoelectronics. However, the increment in wafer-size has not followed the same

progress and there are major concerns about the up-scaling of InP wafer dimensions [78]. InP wafers has several shortcomings, it is fairly immature and the crystal quality is less than the more mature Si and GaAs technologies. InP wafers are more brittle and available only in small sizes (they also carry a price premium US $50/sq. In). By implementing wafer bonding technology Si could be an introduced as a substrate for InP-based materials. Si wafers offers several advantages, it is low-cost, large area, mechanically strong and has high thermal conductivity.

Thermal stress

The closest substitute for heteroepitaxial growth of InP on Si is hydrophobic InP-to-Si direct wafer bonding. Before bonding the native oxide is removed from the surfaces to have a crystal to crystal bonding. HF acid completely removes both Si and InP native oxides [79,80], as was seen also from XPS spectra in this work [paper V]. However the hydrophobic bonding is very weak at room temperature and after low-temperature annealing, because of the hydrogen-terminated surface. A high-temperature annealing above 520 °C is necessary to desorb hydrogen from surface and enable a crystal to crystal covalent bonding. Unfortunately the difference in thermal expansion between InP and Si will induce high mechanical stress in the material ($\alpha_{InP}=4.8\bullet10^{-6}$/K and $\alpha_{Si}=2.6\bullet10^{-6}$/K) when annealing the bonded wafers at high-temperatures. The thermal stress degrades the material by generating defects. It can also make the wafers crack and completely debond, Fig. 12. The main degradation occurs in InP since Si is a mechanically stronger material.

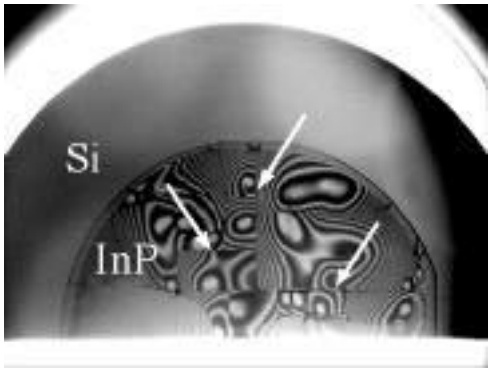

Figure 12. IR-transmission image of InP-to-Si hydrophobic wafer bonding after annealing at 570 °C. Cracks in InP wafer are clearly seen whereas the Si wafer remains intact.

Previous work on heterobonding between GaAs and InP have focused on misfit dislocations that appears at the bonded interface and in a near interface region [42,43]. However, in our work on InP-to-Si wafer bonding we showed that dislocations were formed throughout the entire InP wafer [paper V]. Experimentally it was seen that dislocations were generated in InP only when the bonded wafers

where annealed at high temperatures. Three annealing temperatures were used 125 °C, 350 °C and 570 °C and it was seen that dislocations were generated in InP when the bonded wafers were annealed at 350 °C and 570 °C. No dislocation were formed in the bonded InP and Si wafers annealed at 125 °C. By comparing the thermal stress in InP bonded to Si and the critical stress for dislocation generation in InP it is seen that when annealing the bonded wafers below approximately 300 °C the thermal mismatch stress in InP is not high enough to generate dislocations, Fig. 13.

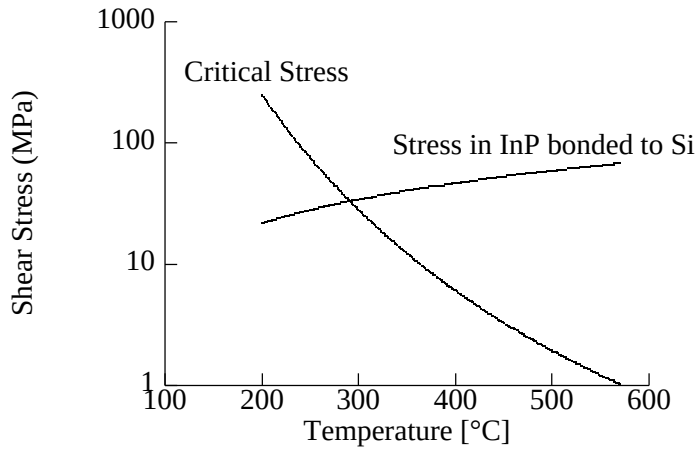

Figure 13. Critical stress for dislocation generation in InP and thermal stress in InP-to-Si wafer bonding. Below the intersection of the curves, which occurs approximately at 300 °C, no dislocations are formed.

Also, when annealing hydrophobic bonded InP and Si wafers above 400 °C macroscopic interface degradation occurred. A set of asymmetric voids started to appear at the interface at 400 °C and as the annealing temperature was increased these asymmetric voids grew in size and number and could cover all the interface when annealing the bonded wafers at 570 °C. These asymmetric voids could occasionally cause complete debonding. When the debonded InP surface was investigated it was seen that the asymmetric voids could be traced to formation of indium droplets and surface steps, Fig. 14. Dislocations sweeping out at the interface locations where micro-cavities are formed are believed to create the surface steps [paper V].

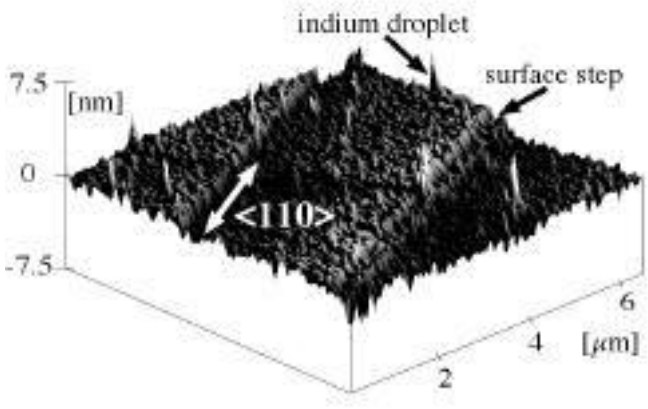

Figure 14. AFM image of an InP surface that debonded from the Si wafers during annealing at 570 °C. Surface step, in <110> direction, and indium droplets are seen.

When an indium droplet is nucleated at the interface it creates a microcavity, hence a 'free' InP surface is obtained at the interface. At the 'free' surface dislocation moving from the InP bulk can sweep out. However, when the Si wafers were patterned with arrays of v-grooves, to create channels at interface, the asymmetric voids completely disappeared. The channels are therefore believed to prevent the nucleation of indium droplets.

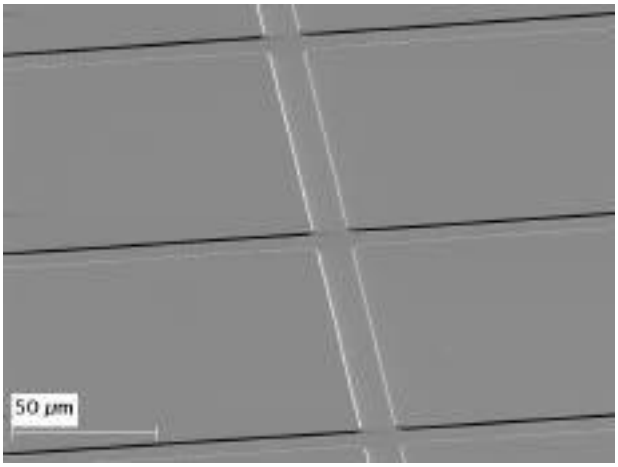

Figure 15. Arrays of channels etched in the Si wafer before bonding.

All in all, the defect study of InP-to-Si hydrophobic wafer bonding proved that compared to results obtained by heteroepitaxial growth of InP on Si, wafer bonding yields a low-defect InP and Si integration technique. However, InP-to-Si wafer bonding was seen not to be a completely defect-free integration technique. Especially the high-temperature annealing and thermal mismatch stress caused both interface degradation and bulk defects to form in InP. To avoid the problems associated with high-temperature annealing and thermal mismatch stress in InP-to-Si wafer bonding it was necessary to develop low-temperature bonding procedures. Low temperature InP-to-Si wafer bonding procedures would further improve bonding yield and the material and interface quality.

Oxygen plasma assisted InP-to-Si wafer bonding

Within this work much effort was made in optimising wafer bonding procedures. Although wafer bonding technology has been used to fabricating devices, the drawbacks and limitations of the wafer bonding technology are seldom discussed, e.g. bonding yield, formation of voids, and degradation. In many wafer bonding reports involving III-V semiconductors chip size wafers are used. Up grading to full wafer-scale bonding puts a more stringent requirement on wafer bonding procedures.

Several wet-chemical pre-treatments were investigated, both hydrophilic and hydrophobic. Using wet-chemical pre-treatments the room temperature bonding of InP and Si always seemed to be non-spontaneous; pressure was required to initiate the bonding. Surface energy measurements showed that the bond-strength started to increase only after annealing at around 400 °C, and even higher annealing temperatures was needed to get a strong InP to Si bonding. The high-temperature annealing and the thermal mismatch stress often made the wafer crack and debond. Especially for full-scale wafer bonding it is also difficult to achieve a uniaxial and uniform load over the entire wafer area during annealing. The uniaxial load is needed when bonding dissimilar material to prevent the wafers from bending.

However, oxygen plasma activation of InP and Si surface was seen to give a very spontaneous bonding at room temperature. After annealing the bonded wafers at temperatures as low as 125 °C and 200 °C the fracture occurred in the InP bulk during crack-opening tests. This indicates the interface strength is equal to, or probably higher then the bulk fracture energy of InP, and therefore the need to anneal the bonded wafers at higher temperatures is very limited. Large-area, full-scale and void-free InP-to-Si wafer bonding was easily realised using oxygen plasma assisted wafer bonding [paper IV].

Oxygen plasma activation was also used for low temperature InP-based epitaxial layer transferring (ELT) to Si substrates [paper VII]. Figure 16 show InP-based LED (light emitting diode) structures on Si. The active structures consist of

InP(p)/InGaAsP (1,55 µm)/InP(n). HRXRD was performed on epitaxial layers after being transferred to Si at 125 °C. The result shows that there was no crystallographic degradation of the InP epitaxial when transferred to Si at these low temperatures. However, as stated previously, oxygen plasma exposure generates a thin surface oxide. Even if this oxide is optically transparent it will increase the junction resistance. Therefore, oxygen plasma wafer bonding procedure is not appropriate for wafer bonding application were low junction resistance is of importance.

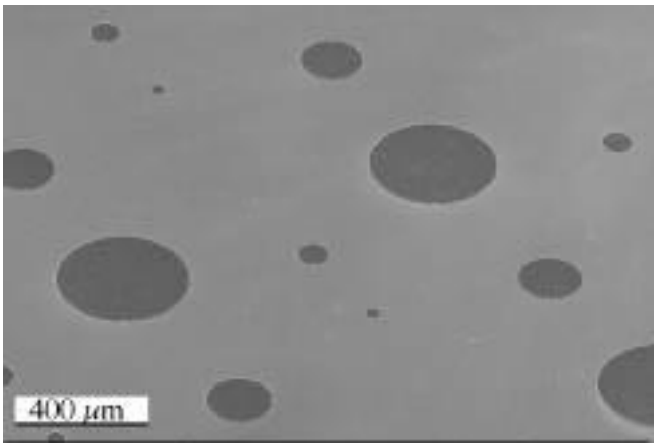

Figure 16. InP-based LED structures on Si substrates. The epitaxial layers were transferred to Si using oxygen plasma wafer bonding and annealing at 125 °C.

Material such as Si forms a high quality Si/SiO_2 structure when oxidised at high temperatures. This is not the case for III-V compound semiconductors. Even if InP has several interesting properties it suffers from the disability of forming high quality oxides during thermal oxidation. A new way of forming InP MOS structures is presented in paper VI. Thermally grown SiO_2 was transferred to InP at low temperatures by oxygen plasma wafer bonding. It was seen that InP MOS structures realised using this technique has several interesting properties compared to previously reported methods for fabrication of InP MOS structures. Figure. 17 shows the C-V curve of InP MOS capacitor fabricated by wafer bonding thermally grown SiO_2 to InP.

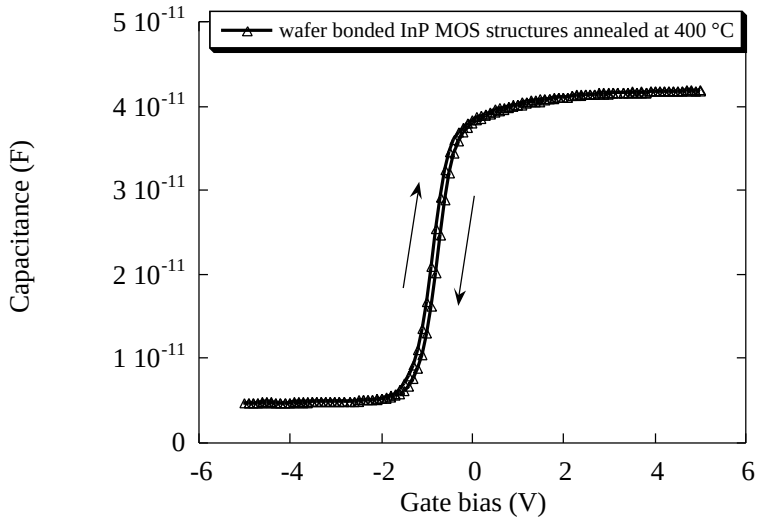

Figure 17. C-V characteristics of InP MOS structure fabricated by transferring thermally grown SiO_2 to InP using oxygen plasma wafer bonding.

5. CONCLUDING REMARKS

It is my belief, and a tendency that I have perceiving, in a very general sense, that the optimal solution does not usually reside in the single material solution but rather in combining disparate materials. This inclination is seen to increase with the demand for increasing devices and system performance. Although more direct approaches such as eutectic bonding, polymer bonding or flip-chip techniques are at hand they may sometimes not be compatible with many specific application, since by their nature they influences interface properties, be it electrical, optical or other. Direct wafer bonding, although having higher constraints regarding its realisation, it poses no such obstacle.

Direct semiconductor wafer bonding has emerged as a tough, front-run competitor to conventional solutions in many high-potential semiconductor applications. But it is my feeling that for the establishment and wider spreading of wafer bonding as a routine procedure, more work is needed in getting standardised, well characterised and defined wafer bonding process, ‘if you do it in this manner the result will be the following…’. An important parameter that is sometimes omitted, is the bonding yield. Through-out this work I have been trying to make a small contribution to the standardisation of wafer bonding procedures.

In this thesis oxygen plasma ‘activation’ of semiconductor surfaces before bonding was used. This proved to be very feasible in achieving a strong bonding already at low temperatures, thereby avoiding the sometime limiting high temperature annealing. It was also seen that in our experimental set-up the results depended on plasma parameters that were used, which is feasible since different plasma parameters gives different surface conditions. Currently, research in wafer bonding using oxygen plasma treatment is also under investigation at other research groups and wafer manufacturer.

Oxygen plasma wafer bonding was also used for the low temperature integration of InP and Si. A high temperature annealing step, as a part of the wafer bonding procedures was seen to induce severe material degradation. Combining the unique features of these material systems is highly sought after and is currently being pursued for several purposes at different research groups.

Even if oxygen plasma assisted wafer bonding produced excellent results, a given extension would be to develop and adapt hydrophobic plasma treatments. Thereby realising a crystal-to-crystal bonding and reducing the junction resistance. This is not within the scope of many wafer bonding applications, on the contrary wafer bonding is often utilised to achieve electrical isolation between bulk quality

semiconductors, with the most prominent example up to this date being SOI wafers. However, for applications where wafer bonding serve e.g. as a direct substitute for epitaxial growth, aimed for application where low junctions resistance is of prime importance, the thin oxide at the interface, resulting from oxygen plasma exposure, may be an obstacle. Therefore, extending the plasma wafer bonding procedures to hydrophobic treatment using e.g. hydrogen plasma, which has been reported to give surface conditions compatible with wafer bonding, both for InP and for Si. A low temperature hydrophobic wafer bonding procedure, enabling crystal-to-crystal bonding of similar or dissimilar semiconductors, would further increase the degree of freedom in e.g. device design, easily realising new materials combinations.

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